**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (canceled)

Claim 2 (new). In a semiconductor memory module divided into banks and having an address structure in which each address is associated with a bank organized in rows and columns and defined with a row address, a column address, and a bank address, a method for comparing a memory access address with a known address of a faulty memory cell, the method which comprises the following steps:

in a first cycle, activating a row by using a row address and a bank address, and during the activation of the row in the first cycle:

comparing the row address with a row address of a faulty memory cell and passing a signal to a latch if an row address match is determined;

comparing the bank address with a bank address of the faulty memory cell; and

obtaining an activation pulse from a rising flank of a bank selection signal by a pulse generator, and passing the activation pulse to the latch if an address match of the bank address with the bank address of the faulty memory cell is determined and an enable register is set; and

in a second cycle, accessing the activated row by using a column address and the bank address, and during the column access in the second cycle:

comparing the column address with the address of the faulty memory cell and passing a signal to a logic stage if a column address is determined; and

outputting a hit signal indicating access to the faulty memory cell by the logic stage, if the bank address match signal, a latch output signal, and the column address match signal are applied to the logic stage, wherein the latch output signal is output to the logic stage by the latch if the activation pulse and the row address match signal are applied to the latch.

Claim 3 (new). In a semiconductor memory module divided into banks and having an address structure in which each address is associated with a bank organized in rows and columns and is defined with a row address, a column address, and a bank address, a part of the semiconductor memory module comprising:

a pulse generator;

a first comparison stage, a second comparison stage, and a third comparison stage;

a latch; and

a first logic stage, a second logic stage, and a third logic stage;

said first comparison stage having a first input receiving a faulty bank address and a second input receiving a bank address;

said second comparison stage having a first input receiving a faulty row address and a second input receiving a row address;

said third comparison stage having a first input receiving a faulty column address and a second input receiving a column address;

said first logic having a first input receiving an output of said first comparison stage and a second input having applied thereto a register set;

said pulse generator having an input receiving a bank selection signal;

said second logic stage having a first input receiving an output of said first logic stage and a second input receiving an output of said pulse generator;

said latching circuit having a first input receiving an output of said second logic stage and a second input receiving an output of said second comparison stage;

said third logic stage having a first input receiving an output of said latching circuit, a second input receiving an output of said first comparison stage, and a third input receiving an output of said third comparison stage.